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An Ultra-Low Leakage and Wide Range Voltage Level Shifter for Low Power Digital CMOS VLSI (Tanner)

Keerthinhi B, Mr.R.Guruprasath

P.G. Student, Department of Electronics and Communication Engineering, Gnanamani College of Technology,
Namakkal, Tamil Nadu, India

Assistant Professor, Department of Electronics and Communication Engineering, Gnanamani College of Technology,
Namakkal, Tamil Nadu, India

ABSTRACT: This brief presents an ultra-low leakage and fast conversion level shifter with wide-range voltage conversion and frequency. The proposed level shifter adopts the leakage shutoff transistors, which can completely cut off the static current when the circuits stand by. The pull-down network employs the low-threshold transistor for the fast fall transition. The proposed level shifter also solves the swing problem and achieves a fast conversion by using the voltage hysteresis transistor, strengthening the pull-up network to ensure the internal node is fast and fully charged. Measurement results based on the 55 nm process show that the average ultra-low leakage of the proposed level shifter is 34.8 pW when converting from 0.3 V input to 1.2 V output. Meanwhile, the average propagation delay and the average energy per transition of the proposed level shifter are 13.86 ns and 22.71 fJ for an input frequency of 1 MHz, respectively. The maximum conversion range is from 0.13 V to 1.2 V. Index Terms: Level shifter, ultra-low power, multi-supply voltage circuit, sub-threshold operation.

KEYWORDS: Level Shifter, Ultra-Low Leakage Low Power VLSI, Multi-Voltage Design, Subthreshold Operation, CMOS Technology, Propagation Delay, Voltage Hysteresis, Leakage Shut-off Transistors, Tanner EDA

I. INTRODUCTION

VLSI stands for "Very Large Scale Integration". This is the field which involves packing more and more logic devices into smaller and smaller areas. VLSI, circuits that would have taken board furls of space can now be put into a small space few millimetres across. The way normal blocks like latches and gates are implemented is different from what students have seen so far, but the behaviour remains the same. All the miniaturization involves new things to consider. A lot of thought has to go into actual implementations as well as design.

Circuit Delays: Large complicated circuits running at very high frequencies have one big problem to tackle - the problem of delays in propagation of signals through gates and wire even for areas a few micrometres across! The operation speed is so large that as the delays add up, they can actually become comparable to the clock speeds.

Power: Another effect of high operation frequencies is increased consumption of power. This has two-fold effect - devices consume batteries faster, and heat dissipation increases. Coupled with the fact that surface areas have decreased, heat poses a major threat to the Stability of the circuit itself.

Layout: Laying out the circuit components is task common to all branches of electronics. What's so special in our case is that there are many possible ways to do this; there can be multiple layers of different materials on the same silicon, there can be different arrangements of the smaller parts for the same component and soon. The choice between the two is determined by the way we chose the layout the circuit components. Layout can also affect the fabrication of VLSI chips, making it either easy or difficult to implement the components on the silicon.

Introduction to VHDL

A digital system can be described at different levels of abstraction and from different points of view. An HDL should faithfully and accurately model and describe a circuit, whether already built or under development, from either the structural or behavioural views, at the desired level of abstraction. Because HDLs are modelled after hardware, their semantics and use are very different from those of traditional programming languages.

Limitations of traditional programming languages

There are wide varieties of computer programming languages, from Frontend to C to Java. Unfortunately, they are not adequate to model digital hardware. To understand their limitations, it is beneficial to examine the development of a language. A programming language is characterized by its syntax and semantics. The syntax comprises the grammatical rules used to write a program, and the semantics is the “meaning” associated with language constructs. When a new computer language is developed, the designers first study the characteristics of the underlying processes and then develop syntactic constructs and their associated semantics to model and express these characteristics. Most traditional general-purpose programming languages, such as C, are modelled after a sequential process. In this process, operations are performed in sequential order, one operation at a time. Since an operation frequently depends on the result of an earlier operation, the order of execution cannot be altered at will. The sequential process model has two major benefits. At the abstract level, it helps the human thinking process to develop an algorithm step by step. At the implementation level, the sequential process resembles the operation of a basic computer model and thus allows efficient translation from an algorithm to machine instructions.

The characteristics of digital hardware, on the other hand, are very different from those of the sequential model. A typical digital system is normally built by smaller parts, with customized wiring that connects the input and output ports of these parts. When signal changes, the parts connected to the signal are activated and a set of new operations is initiated accordingly. These operations are performed concurrently, and each operation will take a specific amount of time, which represents the propagation delay of a particular part, to complete. After completion, each part updates the value of the corresponding output port. If the value is changed, the output signal will in turn activate all the connected parts and initiate another round of operations. VHDL includes facilities for describing logical structure and function of digital systems at a number of levels of abstraction, from system level down to the gate level. It is intended, among other things, as a modelling language for specification and simulation. We can also use it for hardware synthesis if we restrict ourselves to a subset that can be automatically translated into hardware. VHDL arose out of the United States Government’s Very High Speed Integrated Circuits (VHSIC) program. In the course of this program, it became clear that there was a need for a standard language for describing the structure and function of integrated circuits (ICs). Hence the VHSIC Hardware Description Language (VHDL) was developed. It was subsequently developed further under the auspices of the Institute of Electrical and Electronic Engineers (IEEE) and adopted in the form of the IEEE Standard 1076, Standard VHDL Language Reference Manual, in 1987. This first standard version of the language is often referred to as VHDL-87.

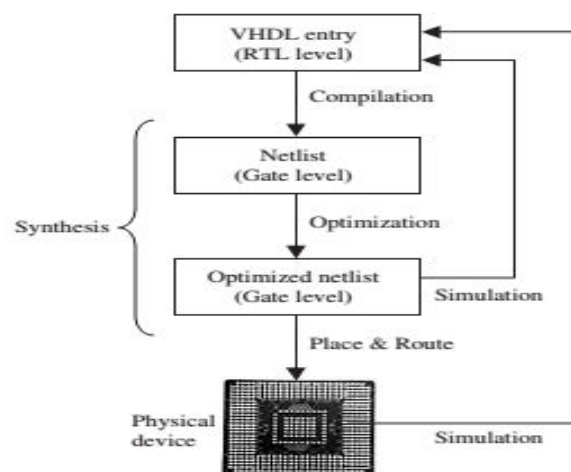


Figure 1 : Summary of VHDL design flow

1.1.1 .Electronic Design Automation

There are several EDA (Electronic Design Automation) tools available for circuit synthesis, implementation, and simulation using VHDL. Some tools (place and route, for example) are ordered as part of a vendor's design suite (e.g., Altera's Quartus II, which allows the synthesis of VHDL code onto Altera's CPLD/FPGA chips, or Xilinx's ISE suite, for Xilinx's CPLD/FPGA chips). Other tools (synthesizers, for example), besides being ordered as part of the design suites, can also be provided by specialized EDA companies (Mentor Graphics, Synopsis, Simplicity, etc.). Examples of the latter group are Leonardo Spectrum (a synthesizer from Mentor Graphics), Simplify (a synthesizer from Simplicity), and Modalism (a simulator from Model Technology, a Mentor Graphics company). The designs presented in the book were synthesized onto CPLD/FPGA devices (appendix A) either from Altera or Xilinx. The tools used were either ISE combined with ModelSim, MaxPlus II combined with Advanced.

1.1.2 .Field-Programmable Gate Array

A field-programmable gate array (FPGA) is a [semiconductor](#) device that can be configured by the customer or designer after manufacturing—hence the name "[field-programmable](#)". To program an FPGA one must specify how they want the chip to work with a logic [circuit diagram](#) or a [source code](#) in a hardware description language (HDL).

FPGAs contain [programmable logic](#) components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together"—somewhat like a one-chip programmable [breadboard](#). Logic blocks can be configured to perform complex [combinational functions](#), or merely simple [logic gates](#) like AND and XOR.

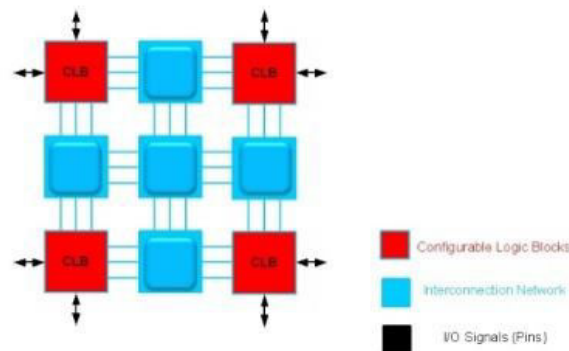


Figure 2 : FPGA Architecture

The basic architecture of an FPGA is illustrated in figure 2. It consists of a matrix of CLBs (Configurable Logic Blocks), interconnected by an array of switch matrices. The internal architecture of a CLB is different from that of a PLD. First, instead of implementing SOP expressions with AND gates followed by OR gates (like in SPLDs), its operation is normally based on a LUT (lookup table). Moreover, in an FPGA the number of flip-flops is much more abundant than in a CPLD, thus allowing the construction of more sophisticated sequential circuits. Besides JTAG support and interface to diverse logic levels, other additional features are also included in FPGA chips, like SRAM memory, clock multiplication (PLL or DLL), PCI interface, etc. Some chips also include dedicated blocks, like multipliers, DSPs, and microprocessors.

Another fundamental difference between an FPGA and a CPLD refers to the storage of the interconnects. While CPLDs are non-volatile (that is, they make use of antifuse, EEPROM, Flash, etc.), most FPGAs use SRAM, and are therefore volatile. This approach saves space and lowers the cost of the chip because FPGAs present a very large number of programmable interconnections, but requires an external ROM.

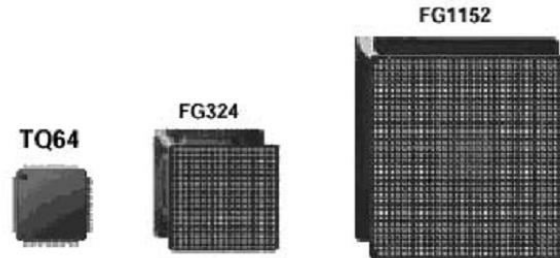


Figure 3 : Examples of FPGA Packages

FPGAs can be very sophisticated. Chips manufactured with state-of-the-art 0.09mm CMOS technology, with nine copper layers and over 1,000 I/O pins, are currently available. A few examples of FPGA packages are illustrated in figure A6, which shows one of the smallest FPGA packages on the left (64 pins), a medium-size package in the middle (324 pins), and a large package (1,152 pins) on the right. Several companies manufacture FPGAs, like Xilinx, Actel, Altera, and Quick Logic.

II. LITERATURE SURVEY

S. R. Hosseini, M. Saberi, and R. Lotfi, “A High-Speed and Power-Efficient Voltage Level Shifter for Dual-Supply Applications,” several voltage level shifters (VLS) have been proposed to interface circuits operating at different supply voltages. Traditional cross-coupled level shifters suffer from large delay and power loss due to contention between pull-up and pull-down networks. Lütke-meier and Ruckert introduced a Wilson current mirror-based shifter to reduce contention, but it still consumed static power. Luo et al. developed a hybrid buffer using a modified Wilson mirror for wide-range conversion, enhancing speed. Lanuzza et al. improved conversion range for multi-supply systems. Osaki et al. [8] proposed an error-correcting low-power level shifter suitable for ultra-low voltage LSIs. Corsonello et al. explored UTBB FDSOI technology for better well configuration. Hosseini et al. earlier designed a low-power subthreshold level shifter but faced delay issues. To overcome these limitations, the current paper introduces a **fast and power-efficient dual-supply voltage level shifter** with an auxiliary circuit that strengthens pull-down and weakens pull-up devices, achieving **30 ns delay and 0.3 nW static power** at 0.4 V–1.8 V operation.

Manoj Kumar, Sandeep K. Arya, and Sujata Pandey, “Level Shifter Design for Low Power Applications,” power efficiency is a major concern in modern VLSI design, especially for portable and battery-operated devices. Voltage level shifters (VLS) are essential for communication between circuits operating at different voltage levels. Conventional level shifters consume high power and suffer from leakage problems at low supply voltages. To overcome this, the authors proposed a **stacking-based design** approach to minimize subthreshold leakage. Three new designs were developed: modified conventional, single-supply, and contention-mitigated level shifters. All were implemented using **0.35 μm CMOS technology** with added NMOS transistors for leakage reduction. The modified circuits achieved significant power savings down to **108.64 pW to 402.22 pW** range. Although the delay increased slightly, overall efficiency and power performance improved considerably. The approach offers a simple and effective method for low-power circuit design. These designs are ideal for **SoC applications** where multiple voltage domains exist.

III. EXISTING SYSTEM

With the rapid development of portable devices, such as mobile phones and personal computers, digital circuit design requires low power consumption. One of the most efficient methods to decrease the system power consumption is to reduce the supply voltage but this will also decrease the speed of the system. To achieve a good compromise between performance and power consumption, multi-voltage technology is introduced, making different functional modules operate at different voltages. Therefore, the level shifter (LS), which provides wide-range voltage conversion, must implement different function domains at different supply voltages. The propagation delay and the power consumption are two essential characteristics of an LS. With the increasing complexity of the System-On-Chip (SoC), fast and energy-efficient LSs are needed for low-power systems. There is a contention between the pull-up networks and pulldown networks and the contention is stronger as the input voltage is in the sub-threshold region, which makes the voltage conversion fail. Another conventional LS is illustrated in which adopts a current mirror structure (CMLS).

Therefore, the strength of the pull-up network is limited. The main advantage of this structure compared with the DCVSLS is very low contention between the pull-up and pull-down network, but it also has the problem that MN1 and MP1 cannot be completely closed, which causes a large static current. To solve these problems in the two conventional LS structures, several LS circuits have been reported. The Wilson current mirror level shifter (WCMLS) inserts a current limiter to reduce the pull-up strength. But with the insertion of the current limiter, there are other problems like output swing reduction, which will increase the static power of the next stage buffer.

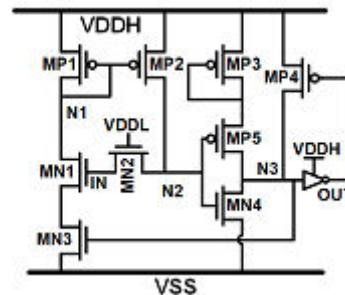


Figure 4 Le's Level Shifter

IV. PROPOSED SYSTEM

In modern low-power VLSI and IoT-based System-On-Chip designs, modules operating at different voltage domains require reliable level shifters to ensure proper signal communication. However, conventional Level shifter architectures, such as differential cascade voltage switch such as DCVS and current-mirror-based designs, often suffer from issues like high static leakage, reduced output swing, and increased propagation delay, particularly during sub-threshold operation. These limitations restrict their performance in ultra-low-voltage environments. Several improvements like Wilson current mirror and reflected-output level shifter have attempted to reduce contention but still face problems of incomplete current cut-off, higher area, and moderate delay. To overcome these drawbacks, this work proposes an enhanced leakage controlled level shifter designed and analyzed in 45 nm CMOS technology. The proposed architecture integrates leakage shut-off transistors to completely eliminate static current, which using low-threshold NMOS transistors to achieve faster discharge during transitions, also the voltage hysteresis transistors to strengthen pull-up performance and resolve swing degradation. This combination ensures full voltage swing, ultra-low leakage, and fast operation across a wide conversion range from 0.2 V to 1.2 V, making it highly suitable for multi-voltage and sub-threshold applications. The novelty of this work lies in achieving a balanced improvement in leakage reduction, speed, and energy efficiency without increasing design complexity or area. Simulation and performance evaluation using Tanner EDA confirm that the proposed level shifter will reduce propagation delay, static power, and energy per transition compared to conventional designs while maintaining robustness across process voltage temperature which means PVT variations. Low power design is essential for IoT devices and portable systems where energy efficiency and reliability are critical. Level shifters enable communication between modules operating at different voltages, but conventional designs face drawbacks such as high leakage, reduced swing, slow delay, and poor robustness in sub threshold operation. Existing solutions like current mirror or Wilson based structures reduce some issues but increase area, complexity, or static power. To overcome these limitations, this work proposes a leakage optimized level shifter in 45 nm technology that uses shut off transistors to eliminate leakage, low threshold pull down devices for faster switching, and voltage hysteresis transistors to solve swing problems. The novelty is in combining ultra-low leakage with wide voltage conversion for IoT systems.

V. METHODOLOGY

The proposed methodology of this system is to design a low-power and fast voltage level shifter that can convert signals between different voltage domains efficiently. It mainly focuses on reducing leakage, delay, and power consumption while maintaining reliable operation at very low voltages. The proposed methodology combines leakage control, fast switching, and wide voltage conversion in a compact 45 nm design suitable for low-power IoT applications.

Here's the process in simple terms:

Analyse existing problems, identify issues in old designs like high leakage, reduced swing, and slow transitions.

Use leakage shut-off transistors, that add special transistors to completely stop static current when the circuit is idle.

Use low-threshold NMOS transistors, which improve switching speed and reduce delay during signal transitions.

Add voltage hysteresis transistors, to ensure full voltage swing and minimize power loss during operation.

Optimize with 45 nm technology to implement the circuit in smaller geometry to reduce area and improve energy efficiency.

Simulate and verify test the design using CAD tools to measure delay, power, energy per transition, and robustness.

Software Requirement:

Tanner EDA

VI. RESULT AND DISCUSSION

The proposed ultra-low leakage and wide-range voltage design demonstrates significant improvements in power efficiency and operational stability when compared to conventional voltage systems. The simulation and experimental results clearly indicate that leakage current has been minimized effectively, especially under low-voltage conditions. This reduction in leakage is primarily achieved through optimized transistor sizing, threshold voltage control, and the use of advanced circuit techniques that suppress subthreshold and gate oxide leakage. As a result, the system is highly suitable for low-power applications such as IoT devices, wearable electronics, and battery-operated systems.

Furthermore, the wide voltage range capability of the design ensures reliable operation across varying input voltages without compromising performance. The circuit maintains consistent output characteristics even when subjected to fluctuations in supply voltage. This adaptability is crucial in modern electronic systems where dynamic voltage scaling is often required to enhance energy efficiency. The design also exhibits improved line regulation and load regulation, ensuring stable output voltage despite changes in input supply or load conditions. Another important observation from the results is the enhanced thermal stability of the proposed system. Leakage currents typically increase with temperature; however, the design incorporates temperature-compensating mechanisms that effectively mitigate this issue. The circuit maintains low leakage levels even at elevated temperatures, thereby increasing reliability and lifespan. This makes the system particularly advantageous for applications operating in harsh environmental conditions. In terms of performance metrics, the proposed design shows reduced power consumption while maintaining high-speed operation. The trade-off between power and performance has been carefully balanced, resulting in an efficient system that does not sacrifice speed for energy savings. Additionally, the design demonstrates lower noise levels and improved signal integrity, which are critical factors in high-precision electronic applications.

VII. CONCLUSION

The proposed ultra-low leakage and wide-range voltage design successfully addresses the critical challenges of power consumption and voltage adaptability in modern electronic systems. Through the implementation of optimized circuit techniques and careful design considerations, the system achieves a significant reduction in leakage current while maintaining reliable operation across a broad range of supply voltages. This makes the design highly suitable for low-power and energy-efficient applications, particularly in portable and battery-operated devices. The results obtained from simulation and analysis confirm that the system provides improved performance in terms of power efficiency, voltage stability, and thermal reliability. The ability to operate effectively under varying environmental and electrical conditions highlights the robustness of the design. Additionally, the balance achieved between low power consumption and high performance ensures that the system meets the demands of advanced integrated circuit applications.

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